IN THE SPECIFICATION:

Please replace paragraph number **[0021]** with the following rewritten paragraph:

[0021] The interposer substrate may be fabricated from a flexible material including a flexible dielectric member, a conductive member, an adhesive on the flexible dielectric member and a solder mask over the conductive member. The flexible dielectric member may comprise a polyimide layer which overlies the solder mask with the conductive member therebetween. The conductive member comprises a pattern of conductive traces formed by etching of a conductive layer carried by the flexible dielectric member or by printing traces on the flexible dielectric member using conductive ink. Trace ends may be enlarged at the intended locations of the recesses to define pads for the terminals and the traces extend therefrom to enlarged bump pads sized and placed for formation of external conductive elements thereon for connection to higher-level packaging. The recesses may be formed through the flexible dielectric member from the surface thereof opposite the conductive member by etching, mechanical drilling or ~~punching~~ punching, or laser ablation, wherein each of the recesses extends to a terminal of a conductive trace and is sized and configured to receive a conductive bump of the semiconductor die. The flexible dielectric member may also optionally include another patterned conductive layer thereon over the surface of the flexible dielectric member to face the semiconductor die. The interposer substrate of the present invention may also be formed of other interposer substrate materials such as a BT resin, FR4 laminate, FR5 laminate and ceramics.

Please replace paragraph number **[0049]** with the following rewritten paragraph:

[0049] It will be observed in FIG. 1 that conductive traces 124 extend over recesses 120 and may optionally extend therebeyond, if desired, for enhanced adhesion of conductive traces 124 to dielectric substrate member 111. Conductive pads or terminals 122 may completely cover the bottoms of recesses 120 or, as depicted in FIG. 1, may be narrower than recesses 120 at the bottoms thereof so that gaps 121 are defined on one or both sides of conductive pads or terminals 122. As implied above, the conductive traces 124, which may, for example, comprise

copper or a copper alloy, may be adhered to the dielectric substrate member of UPILEX®, BT resin, FR 4 ~~or,~~ or FR 5 laminate material, or other substrate materials, using adhesives as known in the art. In some instances, the material of the conductive traces may be adhesively laminated to the dielectric substrate member in the form of a conductive sheet, the traces then being subtractively formed from the conductive sheet, as by etching.

Please replace paragraph number **[0050]** with the following rewritten paragraph:

[0050] Further, interposer substrate 110 may also include an opening 130 (shown in broken lines) formed thereacross, the opening 130 substantially extending along a longitudinal extent of the centrally aligned, single-row configuration of the multiple recesses 120 from one end of interposer substrate 110 to the other. Opening 130 may be formed wholly in the material of dielectric substrate member 111, or may, as shown by the broken lead line from reference numeral 130 in FIG. 2 and the broken lead line from reference numeral 130 in FIG. 3, be formed in solder mask 118. Of course, opening 130 may be formed partially in dielectric substrate member 111 and partially in solder mask 118, as desired. Opening 130 may be formed to align along any employed recess configuration, *i.e.*, ~~I shape~~ I-shaped or peripheral. To better illustrate opening 130, FIG. 2 depicts a cross-sectional view taken along lines 2-2 in FIG. 1. As illustrated, opening 130 includes multiple segments 132, each segment 132 extending between separate individual recesses 120 of the multiple recesses 120. Further, each segment 132 as shown extends along the axis of opening 130 to a side portion of each of the recesses 120; however, the segments 132 may extend and be positioned from the opening 130 to the recesses 120 in any suitable manner. For example, and as depicted in FIG. 1A, opening 130 may comprise a slot laterally offset from recesses 120, which are themselves defined between fingers 111f of flexible dielectric substrate member 111 which terminate at opening 130. As shown, conductive traces 124 extend across opening 130, and solder mask 118 covers the end portions thereof flanking opening 130 and providing an enhanced depth and width to opening 130 for underfilling purposes.

Please replace paragraph number **[0053]** with the following rewritten paragraph:

[0053] FIGS. 4A through 4C depict a process that may be used for forming the recesses 120 in the first surface 112 of interposer substrate 110. FIG. 4A depicts interposer substrate 110 including a dielectric substrate member 111 having a bottom conductive layer formed on a surface thereof and a protective solder mask 118 formed over the conductive layer. The dielectric substrate member 111 is preferably a flexible material, such as the above-described flexible laminated polymer material or polyimide layer, but may also include a substantially nonflexible material. The bottom conductive layer is preferably copper, or a copper alloy, but may be any suitable electrically conductive material. The bottom conductive layer may comprise conductive traces 124 extending between conductive pads or terminals 122 and conductive pads 126 (see FIG. 3). Such conductive traces 124 may be formed by masking and etching a bottom metal or alloy conductive layer or, alternatively, the conductive traces 124 may be formed by printing using conductive ink, or otherwise formed using any method known in the art. Once the conductive traces 124 are patterned, the protective solder mask 118 may be formed thereover.

Please replace paragraph number **[0054]** with the following rewritten paragraph:

[0054] FIG. 4B depicts dielectric substrate member 111 with one of the recesses 120 formed therein. Such recesses 120 may be formed by patterning, utilizing a chemical wet etch or dry etch, mechanical drilling or punching, laser ablation, or any method known in the art and suitable for use with the type of material employed for the dielectric substrate member 111. The recesses 120 are preferably formed to expose portions of one of the conductive traces 124, such as conductive pads or terminals 122. At a bottom of each recess 120 and, for example, at the location of each conductive pad or terminal 122, additional conductive material may be placed, such as gold or eutectic tin/lead solder, the material selected being compatible with the conductive material of the conductive traces 124 and with the bumps of a semiconductor die to be mated with interposer substrate 110. FIG. 4C illustrates that the walls of the recesses 120 may include a conductive layer 123 formed thereon, for example, by electroless plating; however, such plating is not required for practice of the present invention. Further and as shown in

FIGS. 4B and 4C, recesses may be formed with large mouths which taper to a smaller bottom. Such tapering may be easily effected using isotropic etching techniques as known in the art.

Please replace paragraph number **[0055]** with the following rewritten paragraph:

[0055] FIGS. 5A through 5D depict a process similar to that depicted and described in FIGS. 4A - 4C of forming recesses 120 in the first surface 112 of interposer substrate 110, with the addition of another layer, namely, a second conductive layer 125, as shown in FIG. 5A. Such second conductive layer 125 is preferably a copper or copper alloy layer, but may be any suitable electrically conductive material, and may be patterned with traces, depending on the needs and requirements of the particular semiconductor die to which the interposer substrate 110 is attached. FIG. 5B depicts second conductive layer 125 patterned to expose portions of dielectric substrate member 111 where the recesses 120 are to be formed and substantially etched back from the intended lateral boundaries of the recess~~mouths .~~ mouths. As shown in FIG. 5C, a recess 120 is then formed in the exposed portions of dielectric substrate member 111 by a chemical wet etch or dry etch, mechanical drilling or~~punching~~ punching, or laser ablation; however, the recess 120 may be formed utilizing any method known in the art and suitable with the type of material employed for the interposer substrate 110. The recesses 120 are preferably formed to expose conductive pads or terminals 122 of the conductive traces 124, after which additional conductive material may be placed over the exposed portion of the conductive pads or terminals 122. As before, a conductive layer 123 may be formed by electroless plating on the walls of the recesses 120 so that such conductive layer 123 contacts a portion of the conductive pads or terminals 122 of the exposed conductive traces 124, as depicted in FIG. 5D. As shown in FIGS. 5A through 5D in solid lines, solder mask 118 may provide full coverage over the bottoms of conductive traces 124 or, as shown in broken lines, may include an aperture or apertures therethrough, for example, to provide an opening 130 to expose the undersides of conductive traces 124 at the locations of recesses 120 or otherwise, as desired, for enhanced underfill access. If a wet solder mask 118 is employed, recesses 120 in dielectric substrate member 111 are

plugged with a removable material before solder mask application; if a dry (film) solder mask 118 is employed, it may merely be laminated to dielectric substrate member 111.

Please replace paragraph number **[0058]** with the following rewritten paragraph:

[0058] FIG. 6B depicts interposer substrate 110 mounted to semiconductor die 150 to form flip chip-type semiconductor device assembly 160, wherein such semiconductor device assembly 160 provides that each of the conductive bumps 156 is substantially inserted in a corresponding recess 120 of interposer substrate 110 and engages with the conductive pad or terminal 122 at the bottom of each of the recesses 120. Such semiconductor device assembly 160 may be initially attached by the adhesive element 116 carried on the first surface 112 of the interposer substrate 110. The conductive bumps 156 on the semiconductor die 150 may then be bonded to the conductive pads or terminals 122 in the recesses 120 of interposer substrate 110 by, for example, reflowing the conductive bumps 156 (in the case of solder bumps) or curing the conductive bumps 156 (in the case of conductive or conductor-filled polymer bumps) as known in the art. Other methods of bonding known in the art may be utilized, such as ultrasonic or thermal compression.

Please replace paragraph number **[0059]** with the following rewritten paragraph:

[0059] FIGS. 7A - 7B depict simplified cross-sectional views of a second method of mounting and bonding interposer substrate 110 to a semiconductor die 150 in a flip chip-type semiconductor device assembly 160. FIG. 7A illustrates the first surface 112 of interposer substrate 110 aligned with and facing the semiconductor die 150 prior to the assembly thereof. FIG. 7A is similar to FIG. 6A in substantially every respect, except the conductive bumps 156 on the semiconductor die 150 carry a conductive paste 182 thereon. Such conductive paste 182 may be provided on the bumps by dipping the conductive bumps 156 into a pool of conductive paste 182 or by depositing, dispensing or otherwise transferring the conductive paste 182 to the conductive bumps 156. The conductive paste 182 may include, but is not limited to, eutectic solder, conductive epoxy, or any nonsolid conductive material known in the art. As shown,

solder mask 118 may have an opening 130 defined therethrough or, alternatively, full solder mask coverage may be provided across the bottoms of conductive traces 124, including the locations of recesses 120 as previously described with respect to FIGS. 5A through 5D.

Please replace paragraph number **[0060]** with the following rewritten paragraph:

[0060] As depicted in FIG. 7B, the interposer substrate 110 is mounted to semiconductor die 150 to form semiconductor device assembly 160, wherein each of the conductive bumps 156 is substantially inserted into a corresponding recess 120 of interposer substrate 110 with the conductive paste 182 engaging with the conductive pad or terminal 122 in each of the recesses 120. With this arrangement, the conductive paste 182 provides contact with the conductive pads or terminals 122 even if some of the conductive bumps 156 are inconsistent in height, *i.e.*, their free ends are noncoplanar. Such conductive bumps 156 having the conductive paste 182 provided thereon may then be bonded to the conductive pads or terminals 122 in the recesses 120 of interposer substrate 110 as previously described in association with FIGS. 6A and 6B.

Please replace paragraph number **[0062]** with the following rewritten paragraph:

[0062] With the conductive paste 182 in the recesses 120, FIG. 8C depicts the interposer substrate 110 mounted to semiconductor die 150 to form semiconductor device assembly 160, wherein each of the conductive bumps 156 is substantially inserted into the conductive paste 182 in the corresponding recess 120 of interposer substrate 110. As previously described in FIG. 7B, the conductive paste 182 provides electrical and mechanical interconnection between the conductive pads or terminals 122 or trace ends and the conductive bumps 156 even if some of the conductive bumps 156 are inconsistent in height, *i.e.*, their free ends are noncoplanar. The semiconductor die 150 may then be bonded with the interposer substrate 110 as previously described in association with FIGS. 6A and 6B. It will be understood, as noted above, that stencil 186 may not be required if the mass of conductive paste 182 is disposed and spread into recesses 120 prior to disposition of an adhesive

element 116 over first surface 112. Moreover, it will be understood that conductive paste 182, if eutectic solder, may be disposed in recesses 120 and then reflowed and solidified prior to attachment of semiconductor die 150 to interposer substrate 110 using a second reflow to provide an indefinite shelf life for interposer substrate 110. Alternatively, semiconductor die 150 may be aligned with interposer substrate 110 after conductive paste disposition and a single ~~reflow~~ reflow may be employed. FIG. 8D is an enlarged view of a single conductive bump 156 carried by a semiconductor die 150 in initial contact with a mass of conductive paste 182 disposed in a recess 120 in dielectric substrate member 111 of interposer substrate 110 over conductive pad or terminal 122 of a conductive trace 124.

Please replace paragraph number **[0064]** with the following rewritten paragraph:

[0064] FIGS. 9A - 9B depict simplified cross-sectional views of a variant of the above-described third method comprising a fourth method of preparing, mounting and bonding interposer substrate 110 to a semiconductor die 150 in a flip chip-type semiconductor device assembly 160. Such variant is similar to the third method as described in FIGS. 8A - 8D of providing conductive paste 182 in each of the recesses 120, except the conductive bumps 156 are initially unattached to the bond pads 158 of the semiconductor die 150. As depicted in FIG. 9A, the conductive bumps 156 in the form of balls, such as metal balls, are embedded into the conductive paste 182, which was previously spread into the recesses 120 of the interposer substrate 110. The bond pads 158 in the semiconductor die 150 are aligned with the conductive bumps 156 in the recesses 120 in the interposer substrate 110 and then mounted thereto, as depicted in FIGS. 9A - 9B. The conductive paste 182 may comprise a solder wettable to both bond pads 158 and conductive pads or terminals 122 or a conductive or conductor-filled adhesive. It will also be understood and appreciated that conductive bumps 156 may themselves comprise solder, such as a PbSn solder, and conductive paste 182 may be, optionally, eliminated ~~or also comprising a compatible solder~~.

Please replace paragraph number **[0066]** with the following rewritten paragraph:

[0066] It will be well appreciated by one of ordinary skill in the art that, since the bumps are bonded within the recesses 120 of the interposer substrate 110 itself, the height of the flip chip-type semiconductor device assembly 160 is minimized. Therefore, conductive bumps 156 may be formed larger in size than those of conventional flip chip assemblies without increasing, or even while decreasing, the height of the flip chip-type semiconductor device assembly 160, resulting in the increase in electrical and mechanical reliability and performance of the interconnections between the interposer substrate 110 and the semiconductor die 150. Further, the recesses 120 in the interposer substrate 110 provide an inherent alignment aspect absent in a conventional flip chip semiconductor device assembly because the conductive bumps 156 easily slide into their respective corresponding recesses 120 to ensure proper alignment and proper attachment thereof. In addition, the adhesive element 116 on the first surface 112 of the interposer substrate 110 as well as the conductive paste 182 in the recesses 120 may act as a height controller for reliable attachment of the semiconductor die 150 to the interposer substrate 110, wherein the adhesive element 116 and/or the conductive paste 182 may be used to compensate for any irregularities due to varied conductive bump sizes, recess depths and planarity variation in the surfaces of the interposer substrate 110 and semiconductor die 150.

Please replace paragraph number **[0067]** with the following rewritten paragraph:

[0067] As shown in FIG. 10, a dielectric filler material 166 (commonly termed an "underfill" material) may be optionally applied through opening 130. The method employed to apply the dielectric filler material 166 is preferably by dispensing under pressure from dispenser head 164, but may include any method known in the art, such as gravity and vacuum injecting. In this manner, the dielectric filler material 166 may be applied into the opening 130, move as a flow front through the multiple segments 132 and into each of the recesses 120 to fill a space around the conductive bumps 156, bond pads 158 and conductive pads or terminals 122. The dielectric filler material 166 may be self-curing through a chemical reaction, or a cure accelerated by heat, ultraviolet light or other radiation, or other suitable means may be used in order to form

at least a semisolid mass in the recesses 120. Such dielectric filler material 166 provides enhanced securement of the components of flip chip-type semiconductor device assembly 160 as well as precluding shorting between conductive elements and protecting the conductive elements from environmental concerns, such as moisture. As such, compared to the conventional underfilling of the entire semiconductor die, the semiconductor device assembly 160 of the present invention requires less time since the filler material may only be directed to fill the recesses 120 or, rather, any leftover space ~~within in~~ within the recesses 120 proximate the interconnections, *i.e.*, conductive bumps 156.

Please replace paragraph number **[0068]** with the following rewritten paragraph:

[0068] Turning back to the third and fourth methods depicted in FIGS. ~~8A-8D~~ 8A - 8D and ~~9A-9B,~~ 9A - 9B, the interposer substrate 110 described for use in such methods may not include an opening for applying filler material to the recesses 120 because the recesses 120 are substantially filled with conductive paste 182. Therefore, it is contemplated that applying filler material through an opening 130 in the interposer substrate 110 described in the third and fourth methods may not be necessary.

Please replace paragraph number **[0070]** with the following rewritten paragraph:

[0070] FIG. 11 also depicts flip chip-type semiconductor device assembly 160 attached to another carrier substrate 170, such as a printed circuit board or mother board. The carrier substrate 170 includes a substrate upper surface 172 and a substrate lower surface 174, upper surface 172 bearing substrate terminal pads 176 arranged to correspond and attach with conductive balls 162 on the second surface 114 of interposer substrate 110. As such, the flip chip-type semiconductor device assembly 160 may be mechanically and electrically connected to carrier substrate 170 by reflowing the conductive (solder) balls 162 to the substrate terminal pads 176. A dielectric filler material (not shown) as known in the art may then be applied between the flip chip-type semiconductor device assembly 160 and the carrier substrate 170 for securing and protecting the interconnections, *i.e.*, conductive balls 162, therebetween.

Please replace paragraph number **[0071]** with the following rewritten paragraph:

[0071] FIG. 12 depicts a flip chip-type semiconductor device assembly 160 including a heat transfer element 180. The heat transfer element 180 may be provided over the first surface 112 of the interposer substrate 110 and under the adhesive element 116 as a thin, thermally conductive material. The heat transfer element 180 may also be provided on the active surface 152 of the semiconductor die 150 to abut the first surface 112 of the interposer substrate 110. Another option is to provide the heat transfer element 180 on the back side or surface 154 of the semiconductor die 150 as shown in broken lines. Such heat transfer element 180 is configured and located to thermally conduct heat generated from the electrical components of the semiconductor die 150 to remove such heat from the flip chip-type semiconductor device assembly 160 and to reduce the incidence of thermal fatigue in the interconnections and circuitry of the semiconductor device assembly 160 and, specifically, the semiconductor die 150 as well as to reduce operating temperatures. The heat transfer element 180 may be formed of any thermally conductive material, such as copper and silver, but may also comprise a thermally conductive material that is nonelectrically conductive, such as a thin diamond material and/or diamond composite deposited as a thin film or layer.

Please replace paragraph number **[0072]** with the following rewritten paragraph:

[0072] As depicted in FIGS. 13A and 13B, the interposer substrate 110 of the present invention may also be formed initially on a wafer scale corresponding to a semiconductor wafer carrying a plurality of unsingulated semiconductor dice 150 and then singulated or separated after assembly by a dicing process into the individual flip chip-type semiconductor device assemblies 160. As used herein, the term "wafer" is not limited to conventional substantially circular semiconductor wafers but extends to any large-scale substrate including a layer of semiconductor material of sufficient size for formation of multiple dice thereon and encompasses portions of such large-scale substrates bearing multiple semiconductor dice. In particular, FIG. 13A depicts a simplified cross-sectional view of a semiconductor wafer 250 facing a wafer scale interposer substrate 210 prior to mutual attachment thereof. The semiconductor wafer 250

collectively includes multiple semiconductor dice 251 in columns and rows separable along borders 253 as shown in broken lines, wherein the semiconductor wafer 250 includes a back side or surface 254 and an active surface 252 and each semiconductor wafer 250 includes conductive bumps 256 in a configuration dictated by the bond pads on which they are formed.

Please replace paragraph number **[0073]** with the following rewritten paragraph:

[0073] The interposer substrate 210 includes a first surface 212 and a second surface 214 with multiple recesses 220 formed in the first surface 212 and openings 230 having passages (not shown) formed in the second surface 214. The recesses 220 formed in the interposer substrate 210 are made to correspond in substantially a mirror image with the bump configuration on each of the multiple semiconductor dice 251 of the semiconductor wafer 250. In this manner, the interposer substrate 210 may be attached to the semiconductor wafer 250 via an adhesive element 216 on the first surface 212 of the interposer substrate 210 so that the conductive bumps 256 on the semiconductor wafer 250 are inserted into and substantially received within the multiple recesses 220 formed in the interposer substrate 210 to form a wafer scale assembly 260, as depicted in FIG. 13B. The wafer scale assembly 260 may then be singulated or "diced" along the borders 253 of the semiconductor wafer 250 via a dicing member such as a wafer saw 280 to form individual, singulated flip chip semiconductor device assemblies that each include one or more semiconductor dice 251 having the separated interposer substrate 210 of the present invention mounted thereon.

Please replace paragraph number **[0074]** with the following rewritten paragraph:

[0074] Also at the wafer level and as previously described in association with FIGS. 6A-6B, 7A-7B, 8A-8D, and 9A-9B, the conductive bumps 256 may be bonded to the conductive pads or terminals in the recesses 220 to, therefore, mechanically bond and electrically connect the semiconductor wafer 250 to the wafer scale interposer substrate 210. In addition, dielectric filler material may be applied through the openings 230 and conductive balls 262 may

be provided on the bond posts on the second surface 214 of the interposer substrate 210, either prior to dicing the wafer scale assembly 260 or subsequent thereto.

Please replace paragraph number **[0078]** with the following rewritten paragraph:

[0078] Further, in this alternative embodiment, it is preferred that the semiconductor die 450 is assembled and bonded to the interposer substrate 410 with the conductive bumps 456 disposed in the conductive paste 182 as described in FIGS. ~~8A-8D~~ 8A - 8D and ~~9A-9B;~~ 9A - 9B; however, this alternative may also employ the methods described in FIGS. ~~6A-6B~~ 6A - 6B and ~~7A-7B~~ 7A - 7B for assembling and bonding the semiconductor die 450 to the interposer substrate 410.

Please replace paragraph number **[0079]** with the following rewritten paragraph:

[0079] As illustrated in block diagram form in drawing FIG. 17, flip chip-type semiconductor device assembly 160 of the present invention is mounted to a circuit board 570, such as previously discussed carrier substrate 170, in a computer system 500. In the computer system 500, the circuit board 570 is connected to a processor device 572 which communicates with an input device 574 and an output device 576. The input device 574 may be a keyboard, mouse, joystick or any other computer input device. The output device 576 may be a monitor, printer or storage device, such as a disk drive, or any other output device. The processor device 572 may be, but is not limited to, a microprocessor or a circuit card including hardware for processing computer instructions. Additional structure for the computer system 500 is readily apparent to those of ordinary skill in the art.

Please replace paragraph number **[0080]** with the following rewritten paragraph:

[0080] As a further approach to implementing the present invention and as depicted in FIG. 18, an interposer substrate 110 may be provided having conductive traces 124 laminated thereto, the bottoms thereof being fully covered or, optionally, uncovered by solder mask 118, and a conductive bump 156a formed by reflow (if solder) or curing (if an epoxy) of a mass of

conductive paste 182 at the bottom of each recess 120. A dielectric filler material 166~~in~~ is then disposed over conductive bumps 156a in each recess 120 as shown. A semiconductor die 150 carrying a like plurality of conductive bumps 156b arranged for superimposed contact with conductive bumps 156a when semiconductor die 150 is aligned with interposer substrate 110 is then aligned over interposer substrate 110 and vertically pressed thereagainst as depicted by arrow M, the die placement motion squeezing the nondielectric filler material laterally outward so that conductive bumps 156a and 156b meet and make conductive contact. Adhesive elements 116 may, as shown, be used, or may be omitted, as desired.

Please replace paragraph number **[0081]** with the following rewritten paragraph:

[0081] In a variation of the approach of FIG. 18, it is also contemplated that, in lieu of using dielectric filler material 166 and to provide an interposer substrate-to-die adhesive instead of using a separate adhesive element 116, a nonconductive film NCF as shown in broken lines in FIG. 18 be disposed over interposer substrate 110 after formation of conductive bumps 156a thereon and prior to assembly with a semiconductor die 150 carrying conductive bumps 156b. When the semiconductor die 150 and interposer substrate 110 are pressed together, conductive bumps 156a and 156b will penetrate the nonconductive film to initiate mutual electrical contact therebetween. Suitable nonconductive films include the UF511 and UF527 films offered by Hitachi Chemical, Semiconductor Material Division, Japan.

Please replace paragraph number **[0083]** with the following rewritten paragraph:

[0083] The present invention may employ a recess lateral dimension or diameter which is far in excess of the lateral dimension or diameter of an associated conductive bump, thus greatly facilitating bump and recess alignment by loosening required dimensional tolerances. For example, a ~~75μm~~ 75 μm bump may be employed with a 120 μm recess using a 175 μm pitch.